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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional)
X-1505 US

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on November 15, 2007
Signature _____
Typed or printed name Pat Tompkins

Application Number <u>10/777,419</u>	Filed <u>02-12-2004</u>
First Named Inventor <u>Christopher H. Dick</u>	
Art Unit <u>2123</u>	Examiner <u>Andre Pierre Louis</u>

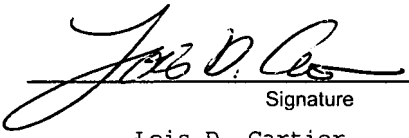
Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

- ☐ applicant/inventor.
- ☐ assignee of record of the entire interest.
See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed.
(Form PTO/SB/96)
- ☐ attorney or agent of record.
Registration number _____
- ☒ attorney or agent acting under 37 CFR 1.34.
Registration number if acting under 37 CFR 1.34 40,941


Signature
Lois D. Cartier
Typed or printed name
720-652-3733
Telephone number
November 15, 2007
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☐ *Total of _____ forms are submitted.

This collection of information is required by 35 U.S.C. 132. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11, 1.14 and 41.6. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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X-1505 US
10/777,419

PATENT
Conf. No.: 4321

IN THE UNITED STATES PATENT OFFICE

Applicants: Christopher H. Dick et al.
Assignee: Xilinx, Inc.
Title: Vector Transfer During Co-Simulation
Serial No.: 10/777,419 File Date: 02-12-04
Examiner: Andre Pierre Louis Art Unit: 2123
Docket No.: X-1505 US Conf. No.: 4321

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PRE-APPEAL CONFERENCE BRIEF

Dear Sir:

This Brief is submitted for the Pre-appeal Conference requested in the Notice of Appeal with which this Brief is submitted.

A. The rejection of claims 1-12, 14-17, and 23 should be withdrawn because the Examiner has not established a *prima facie* case of obviousness of the claims under 35 U.S.C. §103(a) over Lee in view of Cooke.

The Examiner has failed to establish a *prima facie* case of obviousness of these claims over the Lee-Cooke combination because the Office Action does not show that all the limitations are suggested by the combination and does not provide a proper motivation for modifying the teachings of Lee with teachings of Cooke.

According to claim 1, a method for transferring data between blocks in a design during simulation includes "determining a first buffer size in response to specification of a vector input port of a first high-level block of the design; determining a second buffer size in response to specification of a scalar input port of a second high-level block of the design; ... accumulating a plurality of scalar data values received at the scalar input port in a second vector of data values that fills the second buffer size, by the second high-level block..." The second vector of data values is transferred "via a single call to the first function of the interface that couples the HLMS to the second

hardware-implemented block.”

Lee does not in any apparent manner consider the specification of a vector input port or a scalar input port in determining buffer sizes. The claims clearly set forth that the first buffer size is determined in response to specification of a vector input port of a first high-level block of the design, and the second buffer size is determined in response to the specification of a scalar input port of a second high-level block of the design. However, no teachings of Lee in any apparent manner correspond to these specific limitations.

The Examiner generally cites to Lee's pages 152-167 as having teachings that correspond to these limitations. These pages contain source code that implements a wrapper that encapsulates remote processes running in remote machines; a sockPort that accepts a connection request and has an I/O utility for sending and receiving a stream socket; and an interface library for a single board computer using UNIX sockets. Nothing in this source code appears to suggest that buffer sizes are determined based on a specification of a vector input port of a first high-level block of the design and a specification of a scalar input port of a second high-level block of the design. Lee contains no apparent high-level design specification of a vector input port of a block. Nor is there any apparent high-level design specification of a scalar input port of a block. Thus, there is no apparent determining of a buffer size based on the stated specifications of these input ports.

The cited teachings of Cooke do not suggest the limitations of the sizes of buffers used in transferring vectors being determined from the scalar input port and vector input port of high-level design blocks. Cooke's teachings at col. 41-42 are apparently related to designing bus bridges. Thus, there is no apparent suggestion of using the specification of either the scalar input port or the vector input port in high-level design blocks to determine the sizes of the buffers which are used during co-simulation (there being no buffer specified in an actual design created under Cooke).

The asserted motivation for combining Cooke with Lee is unsupported by evidence and improper. The Office Action states that “it would have been obvious ... to combine the simulation method of Cooke et al. with the co-verification system and method of Lee because Cooke et al. teaches the advantage of using a method that

provides a methodology for constructing re-usable circuit blocks which takes account of the special requirements of programmable components, and facilitates the integration of such programmable components with non-programmable components." There is no evidence presented that Lee's system is in any way deficient in the way in which programmable components may be integrated into a design. Nor does the Office Action provide any evidence that shows how specific teachings of Cooke would remedy any of Lee's deficiencies. Therefore, the asserted motivation is improper.

Independent claim 23 is an apparatus claim that includes functional limitations similar to those of claim 1 as discussed above. Claims 2-12 and 14-17 depend from claim 1 and include limitations that further refine the limitations of claim 1 as discussed above. Therefore, the Office Action has not shown that the Lee-Cooke combination suggests the limitations of claims 2-12, 14-17, and 23.

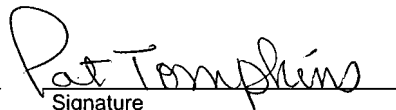
The rejection of claims 1-12, 14-17, and 23 should be withdrawn because a *prima facie* case of obviousness has not been established.

Conclusion

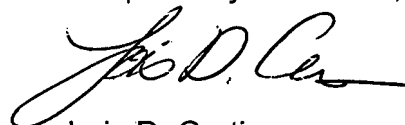
In view of the above, Appellants submit that the rejections are improper, the claimed invention is patentable, and that the rejections of claims 1-12, 14-17, and 23 should be reversed. Appellants respectfully request reversal of the rejections as applied to the appealed claims and allowance of the entire application.

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Pat Tompkins
Name


Signature

Respectfully submitted,



Lois D. Cartier
Agent for Appellants
Reg. No. 40,941